Claims

[c1] 1. A collapsible pipeline structure, suitable for use in a microprocessor, the structure comprising:

a first pipeline stage, under control of a clock to export a sequence of instruction stage results, one result per clock cycle;

a bypassing storage unit, which receives the sequence of instruction stage results from the first pipeline stage and either captures the sequence in a storage unit with respect to the clock and exports the stored output sequence delayed by one clock cycle, or when operating in collapsed mode, exports the sequence of results from the first stage, directly, bypassing the storage unit; and

a second pipeline stage, which receives the output sequence from the bypassing storage unit, and exports a sequence of results for the second instruction stage, under control of the clock,

wherein if the collapsing function of the bypassing storage unit is enabled through the collapse enable signal, then the first and second pipeline stages are collapsed into a single pipeline stage with respect to the clock, exporting a sequence of collapsed instruction stage results that are the aggregate results of the instruction sequence passing through the first and second pipeline stages, in order;

wherein if the collapsing function of the bypassing storage unit is disabled through the collapse enable signal, then the instruction stages function in an uncollapsed mode.

[c2] 2. The collapsible pipeline structure of claim 1, wherein the bypassing storage unit comprises:

a logic gate unit, receiving the clock and a collapse enable signal;

a storage unit, receiving the sequence of instruction stages from the first pipeline stage and exporting a stored content output under controlled by a logic output from the logic gate unit; and

a multiplexer, receiving the sequence of instruction stage results from the first pipeline stage at a first terminal and the stored result sequence from the storage unit at a second terminal, under control by the collapse enable signal to

select one of them as an output of the bypassing storage unit.

[c3] 3. The collapsible pipeline structure of claim 2, wherein the logic gate unit of the bypassing storage unit comprises an AND logic gate.

[c4] 4. The collapsible pipeline structure of claim 2, wherein the logic gate unit and the multiplexer of the bypassing storage unit are designed together, whereby the logic gate unit receives an inverse logic state of the collapse enable signal while the multiplexer receives an original logic state of the collapse enable signal.

[c5] 5. The collapsible pipeline structure of claim 4, wherein the logic gate unit comprises an AND logic gate with an inverter at the terminal for receiving the collapse enable signal.

[c6] 6. The collapsible pipeline structure of claim 2, wherein the storage unit of the bypassing storage unit comprises a flip-flop circuit.

[c7] 7. The collapsible pipeline structure of claim 2, wherein the storage unit of the bypassing storage unit comprises latch circuit.

[c8] 8. The collapsible pipeline structure of claim 2, wherein the multiplexer of the bypassing storage unit is a two-to-one multiplexer.

[c9] 9. The collapsible pipeline structure of claim 1, wherein the number of the instruction stages being collapsed is two.

[c10] 10. The collapsible pipeline structure of claim 1, wherein the first pipeline stage comprises a first storage unit controlled by the clock and a stage-1 logic circuit coupled in series.

[c11] 11. The collapsible pipeline structure of claim 1, wherein the second pipeline stage comprises a stage-2 logic circuit to receive the output from the bypassing storage unit, and a second first storage unit coupled in series after the stage-2 logic circuit and controlled by the clock.

[c12] 12. A method for configuring the collapsible pipeline structure in a microprocessor under control of a clock for executing instructions, the method

comprising:

grouping the pipeline stage by selecting N number of consecutive pipeline stages with respect to the instruction flow through the pipeline as a group, for which bypassing storage units are employed between each of the N pipeline stages of the group, and for each;

collapsing the group as a single stage under control of a clock and with respect to a clock cycle, when the instructions are operated at a low speed least less than or equal to approximately a fraction 1/N times the maximum operation speed of the processor; and

selecting one of the pipeline stages in the corresponding group as an output at the desired clock cycle.

[c13] 13. The method of claim 12, wherein the N number is equal to 2.

[c14] 14. A method for configuring a pipeline structure associating an instruction having a plurality of instruction stages under a collapsing operation mode, the method comprising:

partitioning the pipeline stages into a plurality of collapsible stage groups, each one of the collapsible groups including a plurality of the pipeline stages and is treated as a single stage with respect to a clock cycle.

[c15] 15. The method of claim 14, wherein each one of the collapsible stage groups comprises of two pipeline stages.